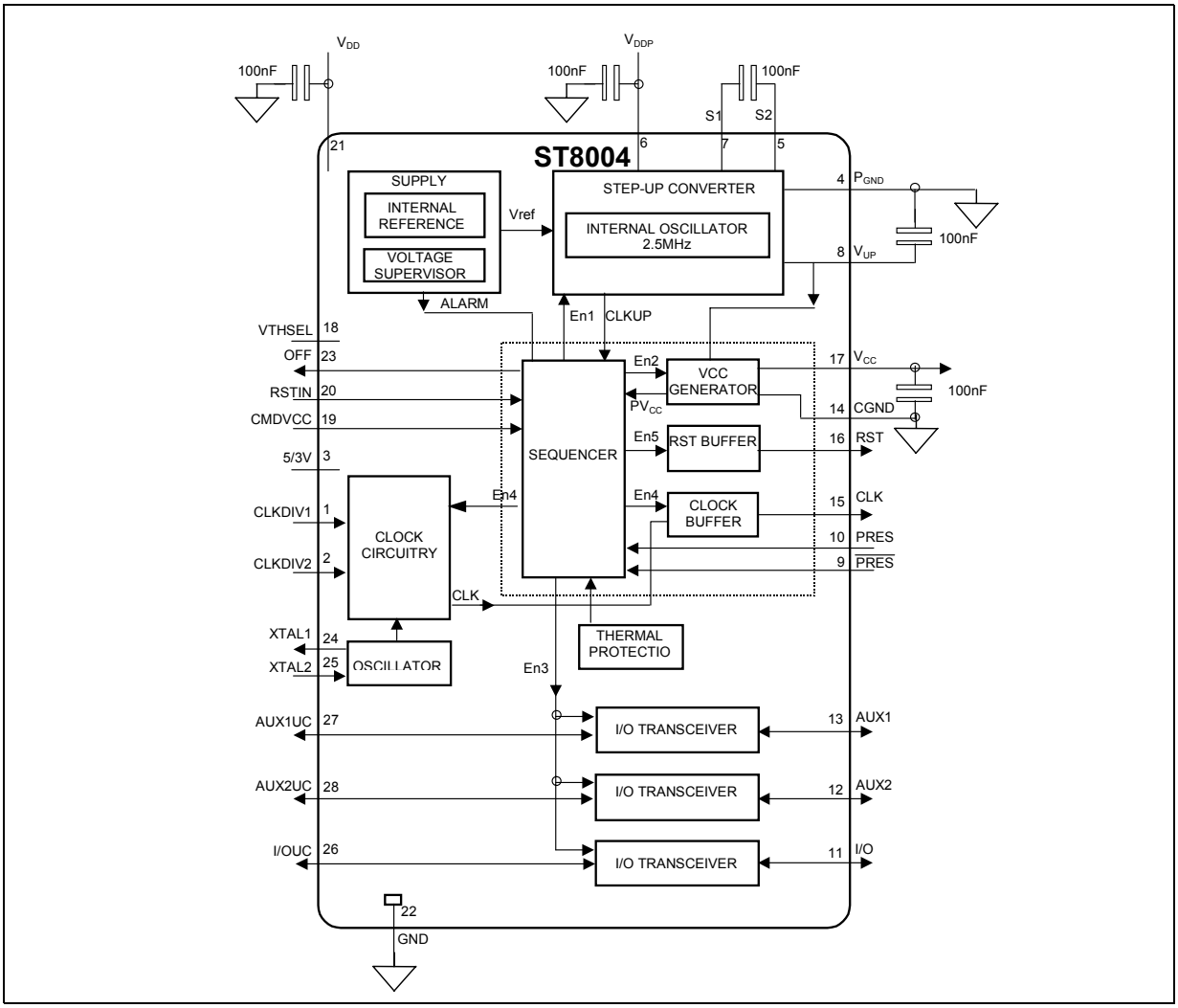
AN1978
APPLICATION NOTE

ST8004: SMART CARD INTERFACE

1. INTRODUCTION

The ST8004 is a smart card interface designed to minimize the microprocessor hardware and software complexity in all the applications that need a smart card, such as Set-Top-Boxes, electronic payments, pay TV and identification.
The ST8004 is compliant with the NDS requirements. It implements all the blocks and procedures for the card activation/deactivation as shown in the block diagram of figure 1.

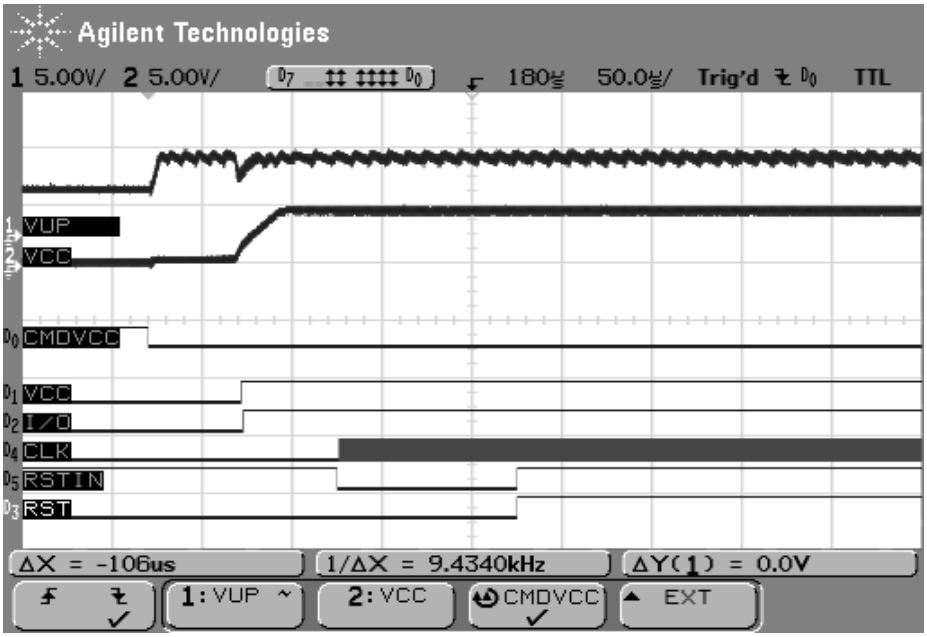
Figure 1: ST8004 internal block diagram



2. SEQUENCER

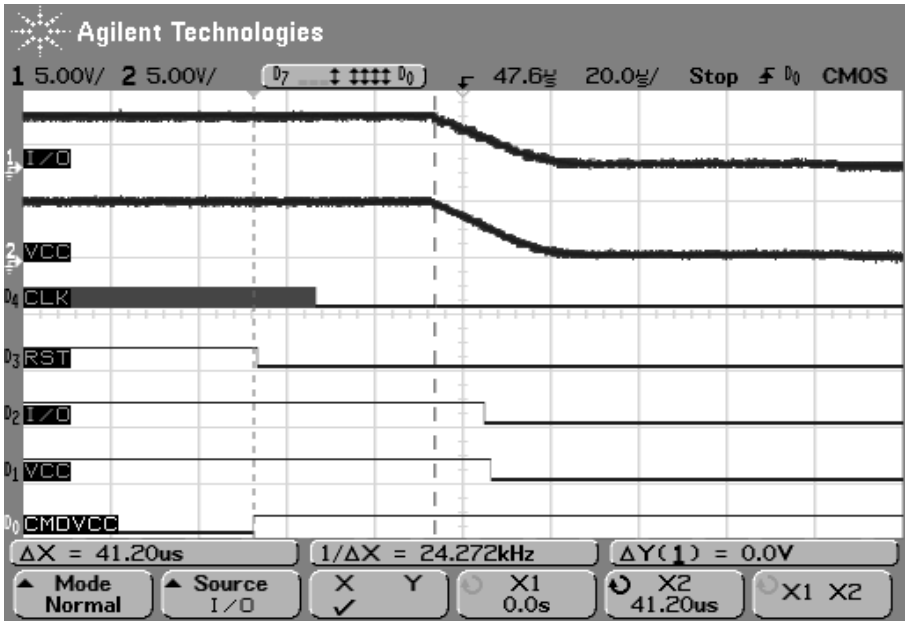
Core of the ST8004 is the sequencer (shown in figure 1) that must coordinate the enable signals for the activation and deactivation sequence and check for possible fault conditions. This because the smart card is basically a microcontroller and needs to be activated/deactivated by a correct sequence as required by the ISO/IEC7816 standard.
Figure 2 and figure 3 show respectively the ST8004 activation and deactivation sequences.

Figure 2: Activation sequence



As shown in figure 2, when the PRES condition is true (PRES = low or PRES = high) and CMDVCC goes low, the activation sequence starts; the first block to be enabled is the step-up converter (V_{UP}), while the last enabled signal is the RST that allows the start of the card software.
Figure 3 shows the deactivation sequence when the CMDVCC goes high. During the deactivation the I/O outputs are deactivated at the time t13 being forced into a three-state condition, following the Vcc slope (see CH 1 in figure 3).

Figure 3: Deactivation sequence



3. CLOCK TO THE CARD

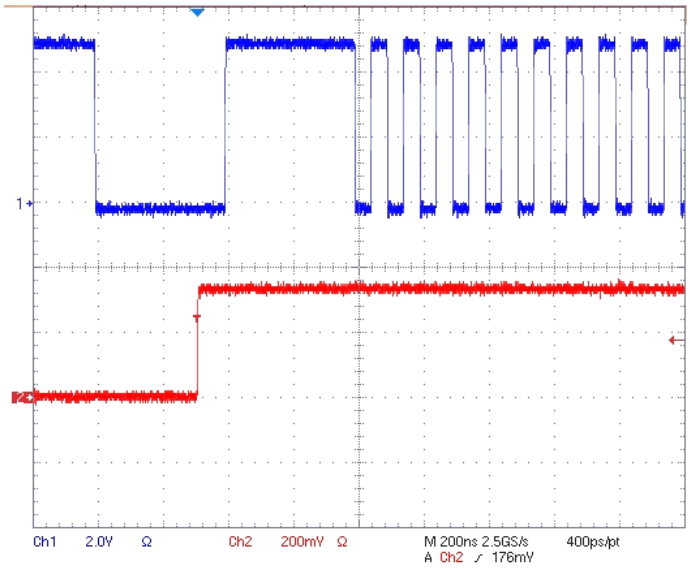
The clock signal to the card is present on the CLK pin when the ST8004 is activated; ; its frequency can be of the same value as one of its ratios compared to the input one (crystal or signal) as shown in the following table (Table 1: CLK division).

Table 1: CLK Division

CLKDIV 1	CLKDIV 2	CLK
0	0	1/8 f_{XTAL}
0	1	¼ f_{XTAL}
1	1	½ f_{XTAL}
1	0	f_{XTAL}

According to the EIA/ISO7816 specifications, the CLK duty cycle must be enclosed between 45% and 55% even if the clock division changes. In this case, at CLKDIV change, the ST8004 waits for the first falling edge to ensure the duty cycle accuracy, as shown in Figure 4.

Figure 4: Clock duty cycle on CLKDIV change



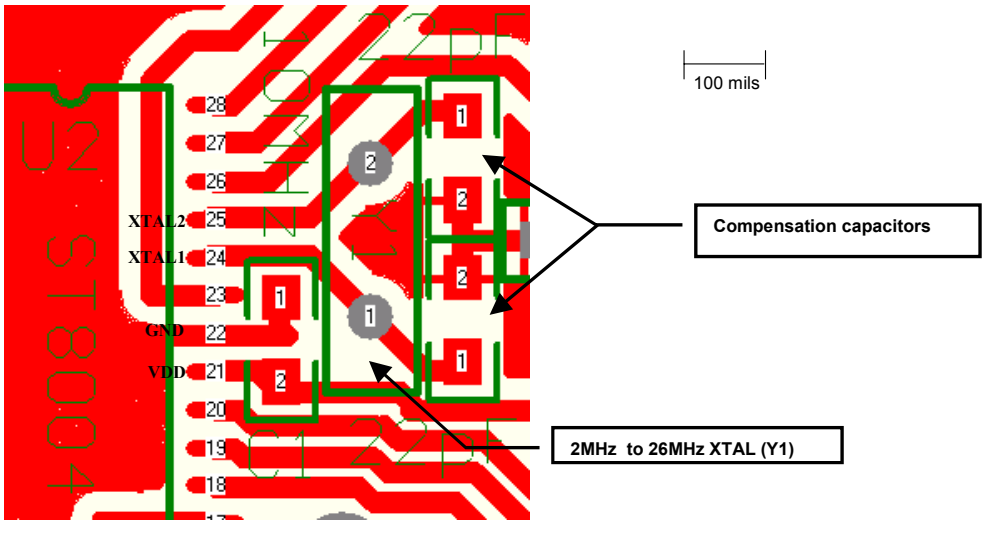
CH1: output CLK waveform.
CH2: CLKDIV1 pin.

Conditions:
VDD=3.3V;
VDDP=5V;
5/3V=H;
CMDVCC=L.
F_{XTAL1}=10MHz;
CLKDIV2=0V;

The output Duty Cycle is 50%±5% even if the Clock Division changes.

The clock signal can be obtained by a crystal connected between the XTAL1 and XTAL2 pins or by an external signal applied to the XTAL1 pin; in this case the XTAL2 pin must be left floating. The external signal voltage value must be enclosed between GND and VDD.
In the PCB design, in order to reduce the reflections especially for the high frequency, the Xtal should be connected as close as possible to the XTAL pins, as shown in figure 5.

Figure 5: XTAL connection



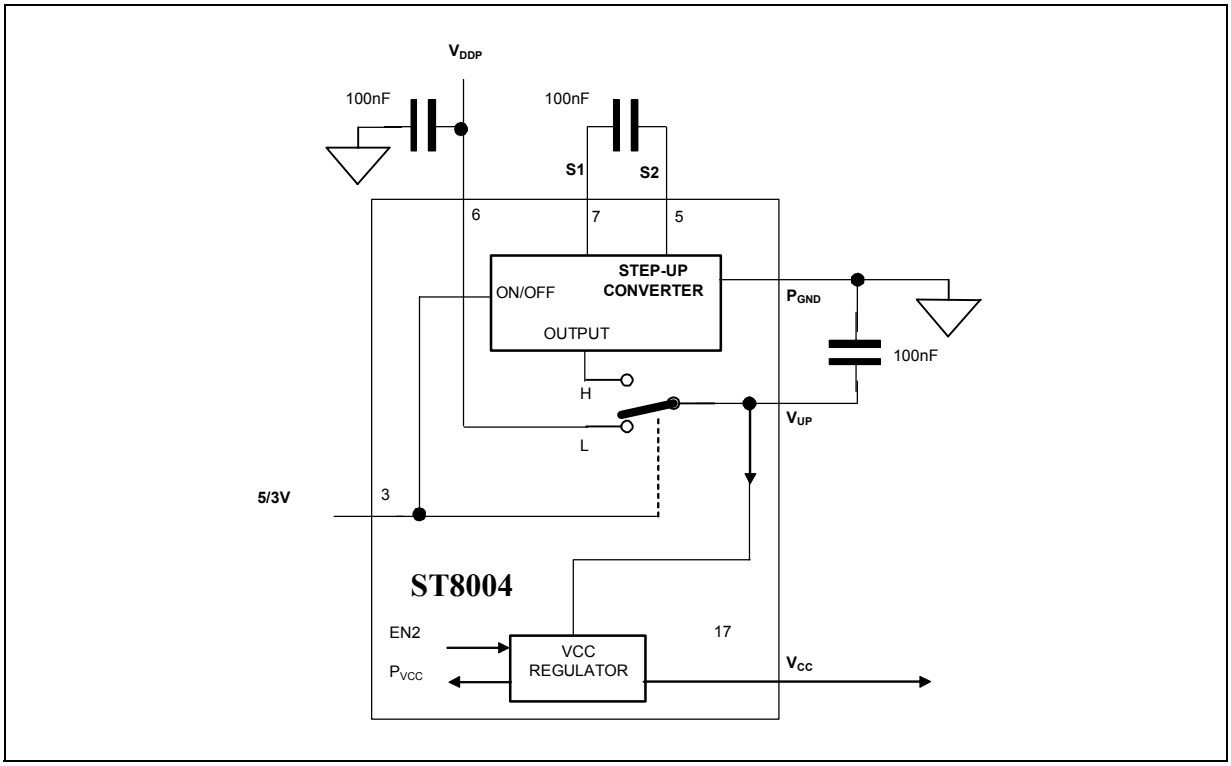
Two compensation capacitors, lower than 22pF, can be used to improve the oscillator performance even if the characterization tests remarked that the CLK Duty Cycle is enclosed between 45% and 55%,

without additional capacitors, even for a frequency higher than 26MHz.
Another recommendation about the CLK output is to keep the CLK wire far from the other signals because inductive or capacitive effects could produce cross conduction on the transceiver lines.
Moreover it is better to shield the clock wire with a ground plain or track on the PCB.

4. STEP-UP CONVERTER AND POWER SUPPLY REGULATOR

The ST8004 can drive both 3V and 5V cards through the supply voltage selector 5/3V pin (pin 3) as shown in Figure 6. If the 5/3V pin is to GND, the Vcc voltage is 3V and the internal Vcc regulator is connected directly to the VDDP pin.
If the 5/3V pin is connected to VDD, the Vcc regulator is connected to the internal step-up converter, as shown in Figure 6, in order to provide the high Vcc supply voltage (5V) even when the VDDP voltage is lower than 5V.

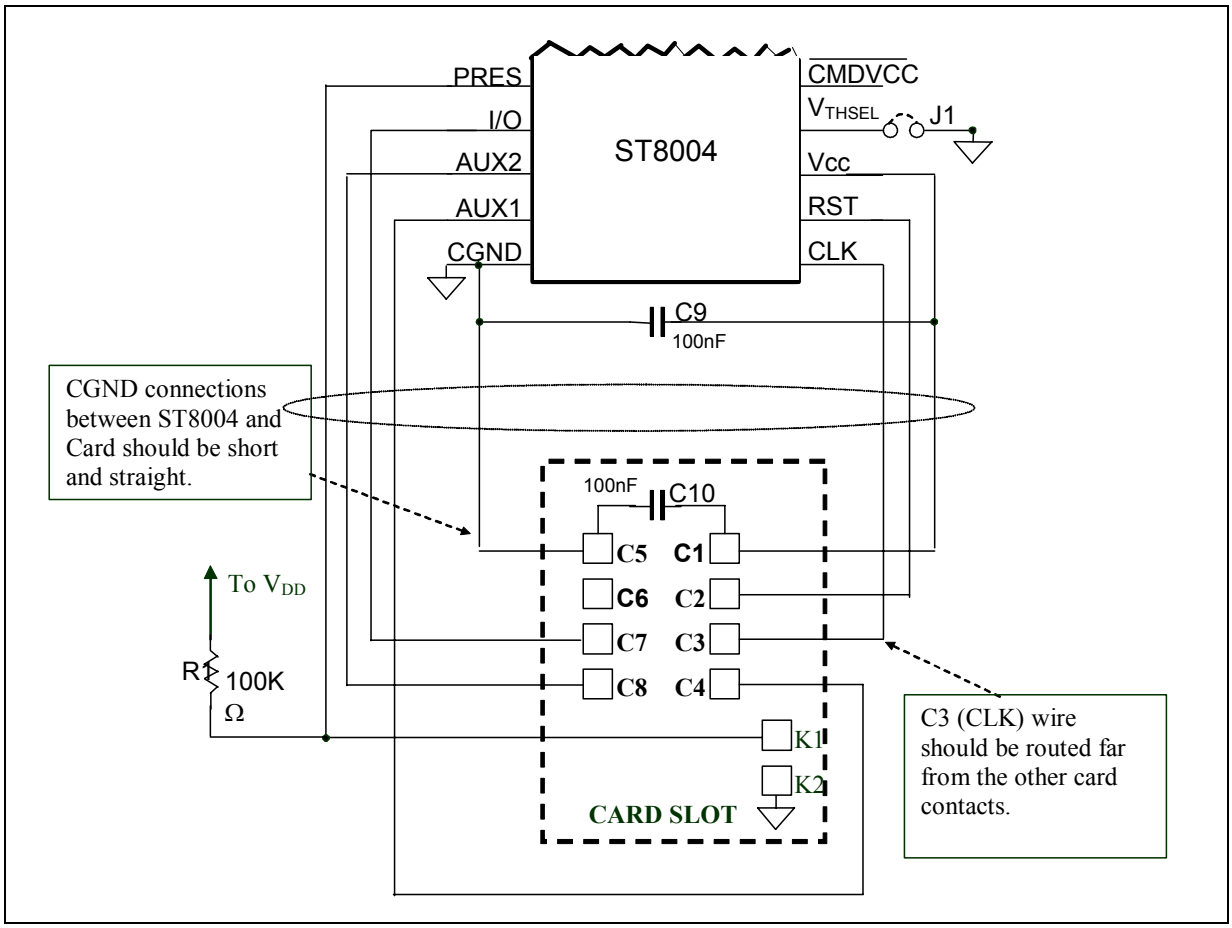
Figure 6: Step-up converter block diagram.



The step-up converter is supplied by the VDDP pin; S1 and S2 pins are used to duplicate the supply voltage through the 100nF pumping capacitor, while the charge pump output is connected to the VUP pin that requires a 100nF storage capacitor to stabilize the voltage.
Due to the switching circuitry, a little noise is introduced so, in order to reduce it and improve the efficiency of the step-up converter, the capacitors must be connected as close as possible to the pins as shown in Figure 9 and are recommended with ESR lower than 50mΩ @ 100kHz such as MURATA GRM31M7U1H104JA01B. Anyway, also capacitor with ESR up to 100mΩ @ 100kHz are enough to work in specifications.

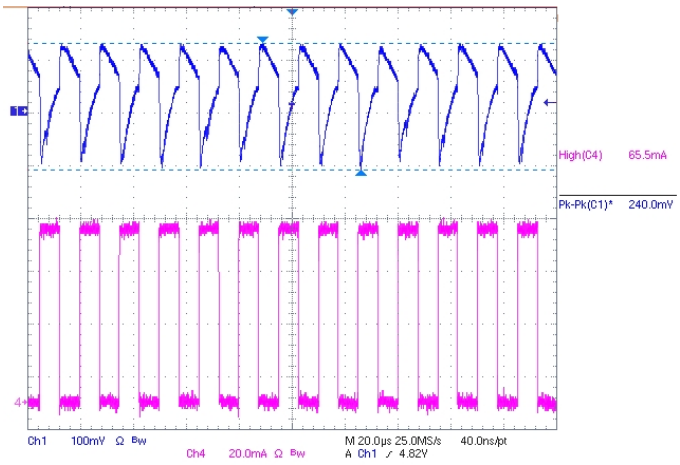
A better noise performance could be achieved connecting the V_{UP} (100nF) capacitor between V_{UP} and V_{DDP} instead of GND. Moreover, a 200nF capacitor should be connected to V_{DDP} into GND in order to obtain a higher current from the charge pump when pulsed load is applied on Vcc.
In the typical applications a 100nF filter capacitor is connected to the Vcc output, near the ST8004 pins and another 100nF is connected, between C1 and C5, near the card slot as shown in Figure 7 and Figure 9. In order to reduce the noise presence and avoid cross conduction effects the wire length between ST8004 and the card should be as short as possible (a wire less than 5cm-long is suggested).
In this way the Vcc spikes are much lower than 350mVpp, even when an impulsive load up to 65mA is applied, as specified in the NDS requirements.

Figure 7: Smart Card connection.



A typical Vcc output waveform, with an impulsive 65mA load applied (worst condition at f=55KHz; D.C.=50%) is shown in Figure 8 where the measured ripple is lower than 240mVpp; the Vcc pin will be able to handle fast current transient generated by the smart card and remain between 4.60V and 5.30V for Class-A and between 2.7V and 3.3V for Class-B (including ripple).

Figure 8: Vcc loaded with a 65mA pulsed current.

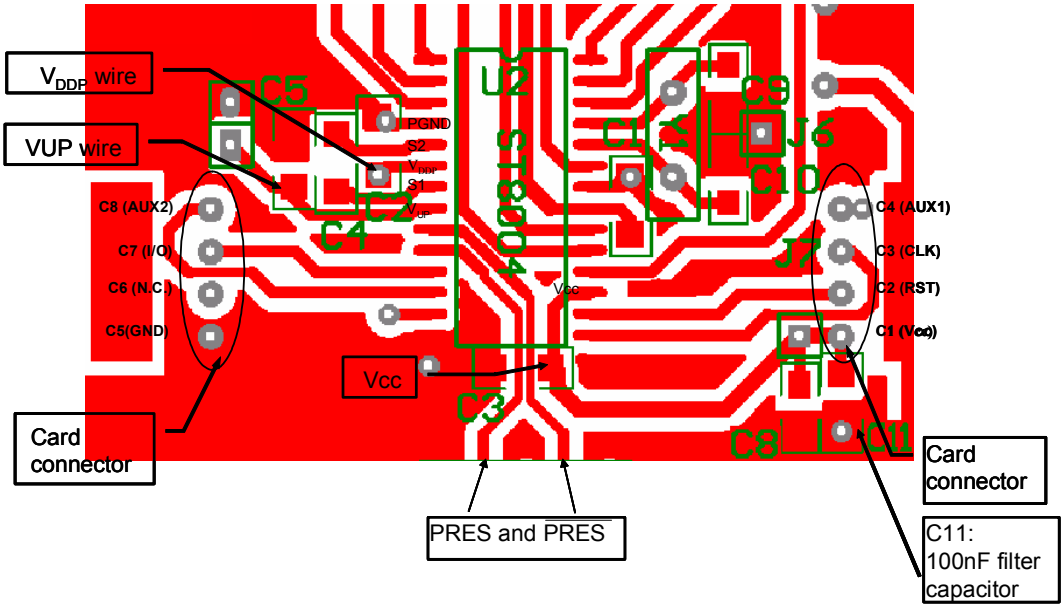


CH1: Vcc voltage; offset=5V; BandWidth=250MHz.
CH4: Vcc output current into GND.

Conditions:
VDD=3.3V;
VDDP=4.75V;
5/3V=H.

The Vcc voltage is between 4.6V and 5.3V even if a 65mA sink pulsed current is forced.

Figure 9: Step-up and Vcc capacitors placement.



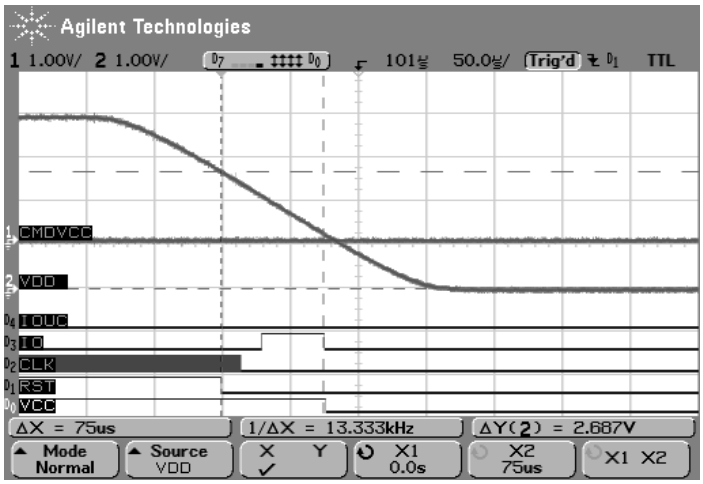
5. FAULT DETECTION

ST8004 provides a fault detection circuitry as shown in Figure 1 monitoring the following conditions:
- Over-temperature detection
- Fault on card removing
- VDD under-voltage
- Vcc Short circuit protection

5.1. VDD under-voltage

The ST8004 logic circuitry is supplied by VDD; in order to avoid voltage spikes causing bad behaviors of device and card, a voltage supervisor block is embedded as shown in Figure 1.
This check block allows the deactivation of the card when the VDD voltage falls below the VTH2 or VTH3 threshold, depending on the VTHSEL selection.
The VTH3 threshold can be used when the microcontroller I/Os continue to work down to 2.85V. In order to provide the correct CLK signal to the card until time t12, the application circuitry should ensure, through filter capacitors, that the VDD voltage falls more slowly than 1.6V/ms. The VDD capacitors used in the evaluation board are 10µF and 100nF.
When the VTHSEL is high or floating and the VDD voltage falls below VTH2, the supervisor starts the deactivation sequence immediately as shown in Figure 13 and the OFF pin goes low (Figure 11).
When the VTHSEL is tied low and the VDD voltage falls below VTH3 for more than about 20µs, the supervisor starts the deactivation sequence as shown in Figure 10.

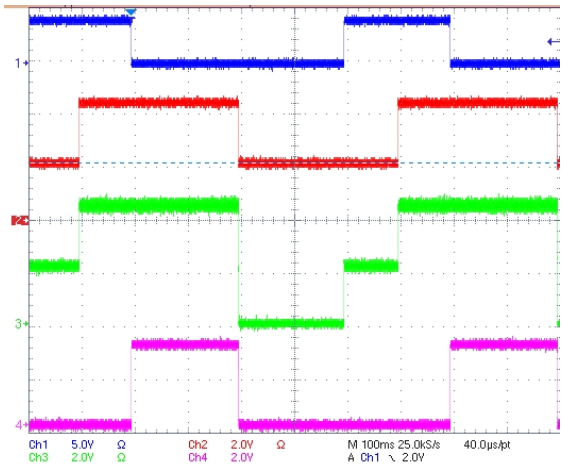
Figure 10: Deactivation sequence when V_{DD} falls down the V_{TH3} voltage



Conditions:
V_{THSEL}= GND;
V_{DD}=4V to 0V;
V_{DD} S.R.=0.015V/µs
V_{DDP}=5V;
5/3V=L.

When the V_{DD} voltage falls below the Vth3 value (about 3.0V in this case) a deactivation sequence starts; after 20µs the RST pin goes low and then the other signals follow the deactivation sequence.

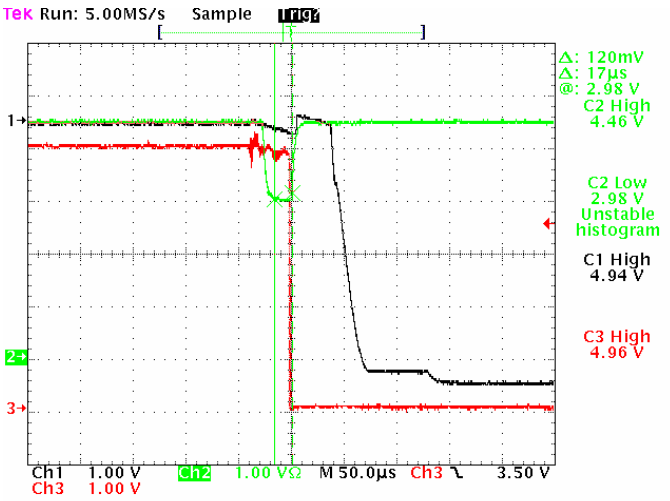
Figure 11: OFF behaviour on VDD drop.



Conditions:
V_{THSEL}= Floating;
V_{DD}=4V to 2V;
V_{DDP}=5V;
5/3V=L.

CH1:CMDVCC
CH2: VDD
CH3: $\overline{OFF}$
CH4: Vcc
When the V_{DD} voltage falls below the Vth2 value (about 2.1V) a deactivation sequence starts and the $\overline{OFF}$ pin goes low until CMDVCC rising edge happens.

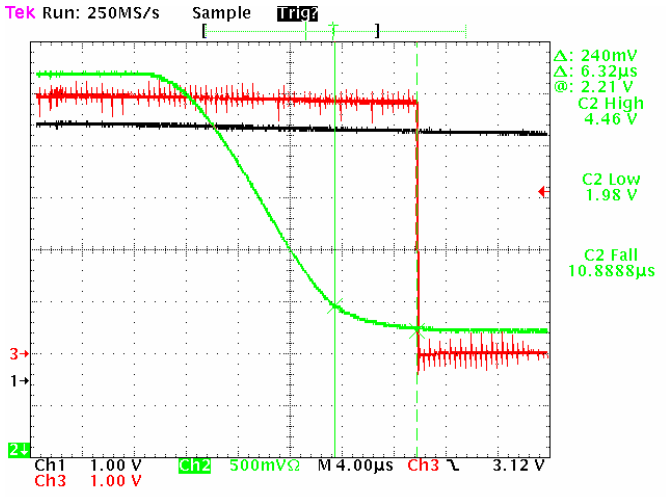
Figure 12: Deactivation sequence automatically when spikes on VDD are present.



Conditions:
V_{THSEL}= GND;
V_{DD}=4.5V to 3V;
V_{DDP}=5V;
5/3V=H.
CH1: Vcc
CH2: V_{DD}.
CH3: RST pin.

When the V_{DD} voltage falls down the Vth3 value (about 3.0V) for more than 20µs. a deactivation sequence starts; the RST pin (CH3) is the first that goes low.

Figure 13: Vth2 threshold.



Conditions:
V_{THSEL}= V_{DD} or floating;
V_{DD}= 4.5V to 2V;
V_{DDP}=5V;
5/3V=H.
CH1: Vcc
CH2: V_{DD}.
CH3: RST pin.

When the V_{DD} voltage falls below the Vth2 value (about 2.1V) a deactivation sequence starts; the RST pin (CH3) is the first to go low after about 6µs.

5.2. Vcc short-circuit protection

An important feature of the voltage regulator is the short-circuit protection that warns the sequencer block (see Figure 1) if the output current grows more than the short circuit current limit (about 90mA). In this case a deactivation sequence starts to protect the card and the OFF pin falls down warning the occurred fault as shown in Figure18. The following figures (Figure 14 and Figure 15) show the load curve of the ST8004 Step-up converter and regulator.
As specified in the NDS electrical requirements the ST8004 is able to maintain the Vcc voltage included in the range 4.75V÷5.25V for the Class-A and 2.80V÷3.20V for the Class-B with current load from 0 to the short-circuit current.
An example of short circuit protection intervention is shown in Figure 16, in which the activation sequence starts in presence of a Vcc short circuit and the protection acts at the end of the activation sequence.
If the short circuit condition happens when the device is already activated, the protection acts immediately as shown in Figure 17.

Figure 14: Vup load curve

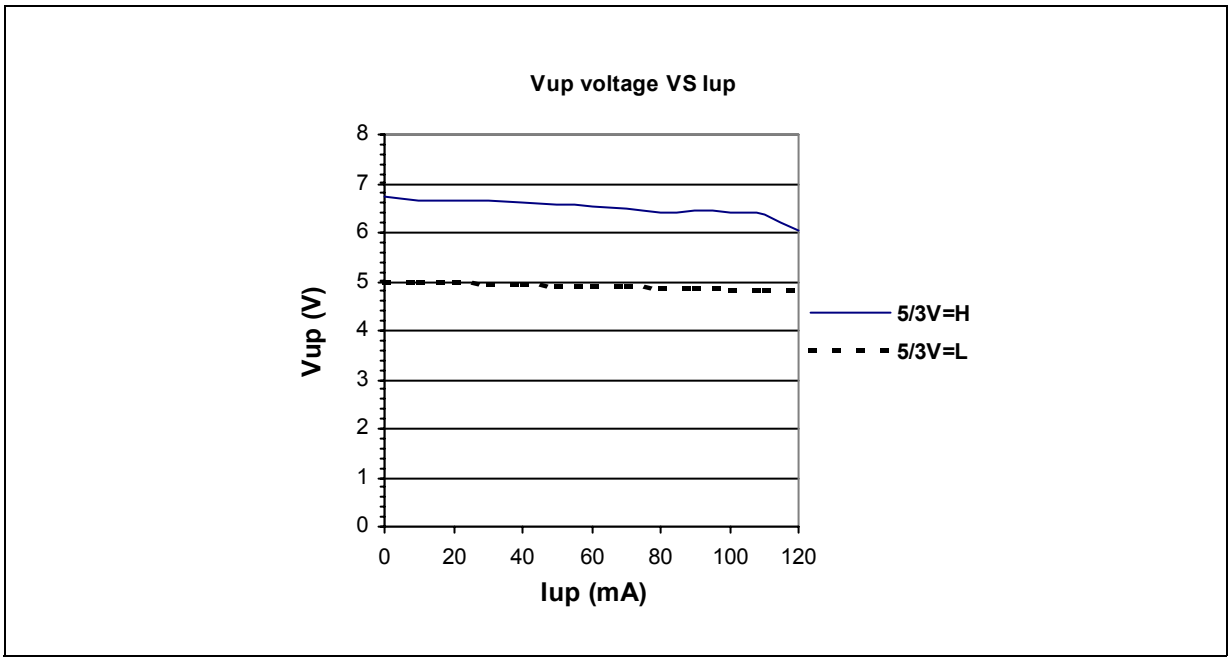


Figure 15: Vcc load curve

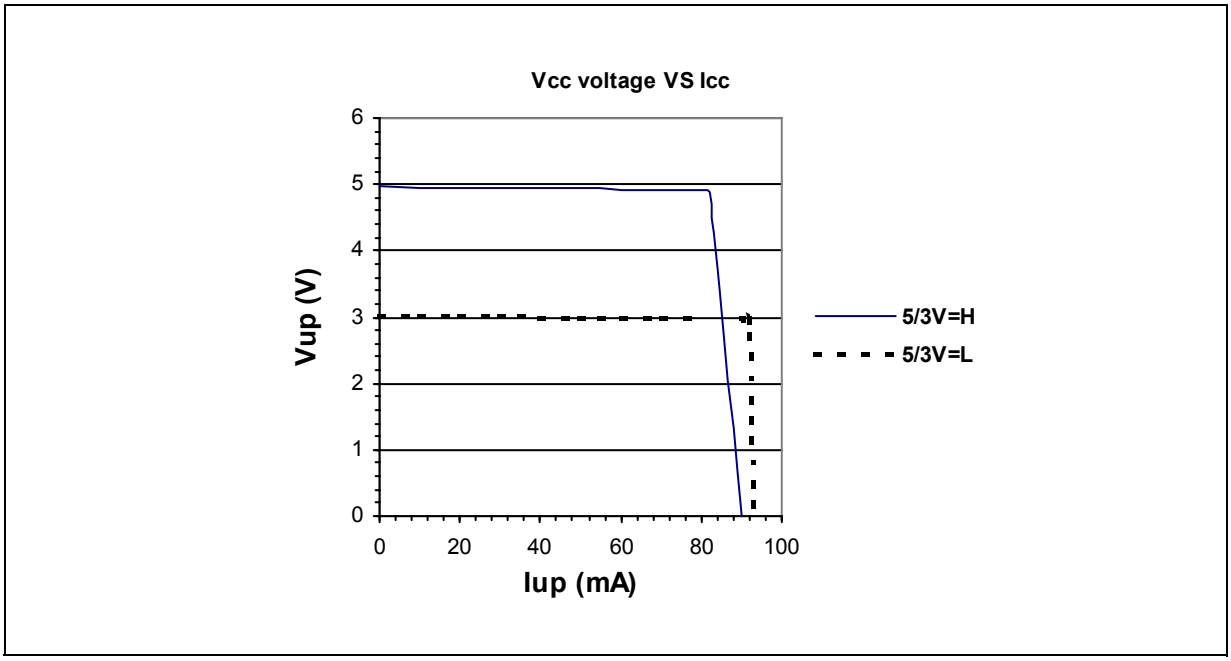
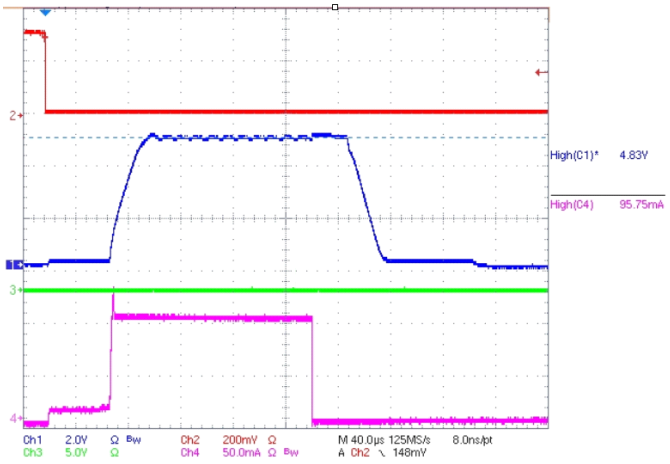


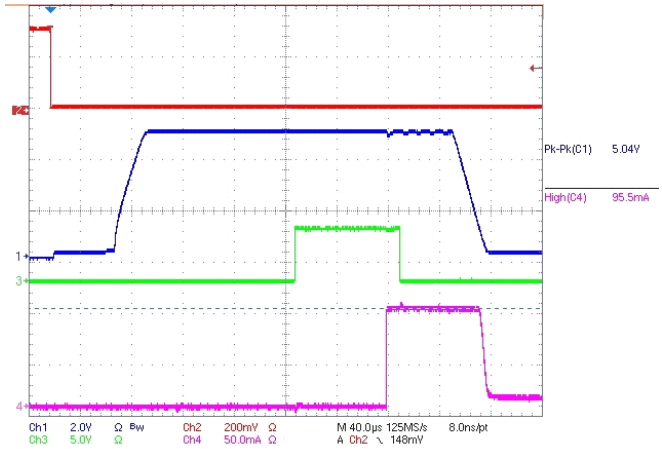
Figure 16: Short-circuit on Vcc during the activation.



Conditions:
V_{DD}= 3V
V_{DDP}=4.75V;
5/3V=H.
CH1: Vcc
CH2: CMDVCC.
CH3: RST .
CH4 : Vcc output current

In this case the short circuit is present before and during the activation sequence, then the automatic deactivation starts as soon as the fault is acknowledged.

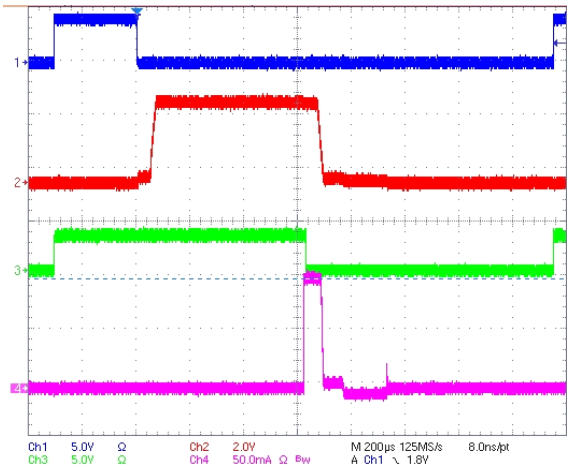
Figure 17: Short-circuit on Vcc after the activation.



Conditions:
V_{DD}= 3V
V_{DDP}=4.75V;
5/3V=H
CH1: Vcc
CH2: CMDVCC.
CH3: RST .
CH4 : Vcc output current

In this case the short circuit acts after the activation sequence then the automatic deactivation starts after about 8µs.

Figure 18: OFF behavior on Vcc short-circuit.



Conditions:
V_{DD}= 3V
V_{DDP}=5V;
5/3V=L
CH1: CMDVCC.
CH2: Vcc
CH3: OFF .
CH4 : Vcc output current

When the short circuit occurs the $\overline{OFF}$ pin goes low indicating a fault.

6. REVISION HISTORY

Table 2: Revision History

Date	Revision	Description of Changes
10-June-2004	1	First Release

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics.
All other names are the property of their respective owners

© 2004 STMicroelectronics - All rights reserved

STMicroelectronics GROUP OF COMPANIES
Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States
www.st.com